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(FILE 'USPAT' ENTERED AT 10:27:05 ON 23 OCT 91)
L1 10 S WRITE BACK CACHE
L2 172 S (DISK DRIVE#) AND CACHE
L3 7 S L2 AND (FAULT TOLERANT)

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1. 5,045,996, Sep. 3, 1991, Multiprocessor cache memory housekeeping; Richard M. Barth, et al., 364/200, 243, 243.4, 243.41, 243.44 [IMAGE AVAILABLE]

US PAT NO: 5,045,996 [IMAGE AVAILABLE] L7: 1 of 27
DATE FILED: Nov. 15, 1989

2. 5,043,886, Aug. 27, 1991, Load/store with write-intent for write-back caches; Richard T. Witek, et al., 364/200, 228.1, 228.3, 243.4, 243.41, 243.44 [IMAGE AVAILABLE]

US PAT NO: 5,043,886 [IMAGE AVAILABLE] L7: 2 of 27
DATE FILED: Sep. 16, 1988

3. 5,038,277, Aug. 6, 1991, Adjustable buffer for data communications in a data processing system; Barbara H. Altman, et al., 364/200, 238.4, 238.6, 239, 239.7 [IMAGE AVAILABLE]

US PAT NO: 5,038,277 [IMAGE AVAILABLE] L7: 3 of 27
DATE FILED: Jan. 12, 1990

4. 5,029,070, Jul. 2, 1991, Coherent cache structures and methods; Daniel M. McCarthy, et al., 364/200, 228.1, 228.3, 243, 243.4, 243.41 [IMAGE AVAILABLE]

US PAT NO: 5,029,070 [IMAGE AVAILABLE] L7: 4 of 27
DATE FILED: Aug. 25, 1988

Matick, et al., 365/189.04, 230.05

US PAT NO: 4,577,293 L7: 22 of 27
DATE FILED: Jun. 1, 1984

23. 4,525,780, Jun. 25, 1985, Data processing system having a memory using object-based information and a protection scheme for determining access rights to such information; Richard G. Bratt, et al., 364/200, 228.3, 231.4, 231.6, 243, 244, 244.3, 246.6, 262.4, 262.8, 263, 286, 286.4, 286.5 [IMAGE AVAILABLE]

US PAT NO: 4,525,780 [IMAGE AVAILABLE] L7: 23 of 27
DATE FILED: May 31, 1984

24. 4,493,027, Jan. 8, 1985, Method of performing a call operation in a digital data processing system having microcode call and return operations; Lawrence H. Katz, et al., 364/200, 228.2, 228.5, 241.2, 244, 244.3, 247, 247.7, 256.3, 258, 260, 260.1, 261.3, 262.4, 262.7, 262.8, 270.5, 280.4 [IMAGE AVAILABLE]

US PAT NO: 4,493,027 [IMAGE AVAILABLE] L7: 24 of 27
DATE FILED: May 22, 1981

25. 4,455,602, Jun. 19, 1984, Digital data processing system having an I/O means using unique address providing and access priority control techniques; Ward Baxter, III, et al., 364/200, 228.1, 228.3, 231.4, 231.6, 232.1, 243, 243.3, 244, 244.3, 246.6, 262.4, 262.8, 263, 280, 280.4, 281.3, 281.4 [IMAGE AVAILABLE]

US PAT NO: 4,455,602 [IMAGE AVAILABLE] L7: 25 of 27
DATE FILED: May 22, 1981

26. 4,445,177, Apr. 24, 1984, Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions; Richard G. Bratt, et al., 364/200, 228.3, 231.4, 231.6, 232.1, 238.4, 239, 239.7, 241.2, 241.3, 241.5, 241.9, 243, 243.4, 243.41, 243.43, 244, 244.3, 244.6, 246.6, 246.7, 246.8, 246.9, 246.91, 247, 247.2, 247.7, 247.8, 254, 254.3, 254.5, 256.8, 258, 258.2, 258.3, 259, 259.5, 259.8, 261.3, 261.6, 262.4, 262.7, 262.8, 262.81, 263, 263.2, 263.3, 265, 265.3, 266, 266.1, 267, 267.6, 267.9, 270, 270.1, 271, 271.3, 271.4, 271.6, 271.8, 280, 280.1, 280.4, 280.8, 280.9, 281, 281.3, 281.4, 281.5, 281.6, 281.7, 281.8, 282, 282.1, 282.2, 284, 284.3 [IMAGE AVAILABLE]

US PAT NO: 4,445,177 [IMAGE AVAILABLE] L7: 26 of 27
DATE FILED: May 22, 1981

27. 4,399,503, Aug. 16, 1983, Dynamic disk buffer control unit; Kenneth R. Hawley, 364/200, 228.3, 236.2, 238.4, 239, 239.4, 239.5, 239.6, 240, 240.1, 241.9, 242.3, 242.31, 242.32, 243, 243.2, 243.3, 243.4, 243.41, 246, 246.1, 246.11, 246.12, 248.1, 248.3, 252, 252.1, 254, 254.3, 254.5, 255.1, 255.7, 260, 260.3, 262.4, 262.6, 262.7, 270.5, 270.7, 271 [IMAGE AVAILABLE]

US PAT NO: 4,399,503 [IMAGE AVAILABLE] L7: 27 of 27
DATE FILED: Jun. 30, 1978

5. 5,025,421, Jun. 18, 1991, Single port dual RAM; Gyung Y. Cho, 365/230.05, 189.04, 228 [IMAGE AVAILABLE]

US PAT NO: 5,025,421 [IMAGE AVAILABLE] L7: 5 of 27
DATE FILED: Jan. 2, 1990

6. 5,007,027, Apr. 9, 1991, Data protection system in a data processing system; Hiroyuki Shimoi, 365/229 [IMAGE AVAILABLE]

US PAT NO: 5,007,027 [IMAGE AVAILABLE] L7: 6 of 27
DATE FILED: May 9, 1989

7. 5,003,463, Mar. 26, 1991, Interface controller with first and second buffer storage area for receiving and transmitting data between I/O bus and high speed system bus; Richard W. Coyle, et al., 364/200, 228.5, 238, 238.3, 239, 239.4, 239.6, 239.7, 240, 240.3, 251.3, 270.2 [IMAGE AVAILABLE]

US PAT NO: 5,003,463 [IMAGE AVAILABLE] L7: 7 of 27
DATE FILED: Jun. 30, 1988

8. 4,995,041, Feb. 19, 1991, Write back buffer with error correcting capabilities; Ricky C. Hetherington, et al., 371/40.1; 364/200 [IMAGE AVAILABLE]

US PAT NO: 4,995,041 [IMAGE AVAILABLE] L7: 8 of 27
DATE FILED: Feb. 3, 1989

9. 4,985,829, Jan. 15, 1991, Cache hierarchy design for use in a memory management unit; Satish M. Thatte, et al., 364/200 [IMAGE AVAILABLE]

US PAT NO: 4,985,829 [IMAGE AVAILABLE] L7: 9 of 27
DATE FILED: Jun. 26, 1987

10. 4,977,498, Dec. 11, 1990, Data processing system having a data memory interlock coherency scheme; Joseph Rastegar, et al., 364/200, 238.4, 243.4, 243.41, 246.8, 900, 964.2, 968, 969.2 [IMAGE AVAILABLE]

US PAT NO: 4,977,498 [IMAGE AVAILABLE] L7: 10 of 27
DATE FILED: Apr. 1, 1988

11. 4,959,777, Sep. 25, 1990, Write-shared cache circuit for multiprocessor system; Thomas H. Holman, Jr., 364/200, 229.2, 243.43, 243.44, 264.5 [IMAGE AVAILABLE]

US PAT NO: 4,959,777 [IMAGE AVAILABLE] L7: 11 of 27
DATE FILED: Jul. 27, 1987

12. 4,941,088, Jul. 10, 1990, Split bus multiprocessing system with data transfer between main memory and caches using interleaving of sub-operations on sub-busses; Stephen J. Shaffer, et al., 364/200, 240.2, 243.43, 243.44 [IMAGE AVAILABLE]

US PAT NO: 4,941,088 [IMAGE AVAILABLE] L7: 12 of 27
DATE FILED: Feb. 5, 1985

13. 4,939,641, Jul. 3, 1990, Multi-processor system with cache memories; Martin J. Schwartz, et al., 364/200, 243.4, 243.41, 259.2 [IMAGE AVAILABLE]

US PAT NO: 4,939,641 [IMAGE AVAILABLE] L7: 13 of 27
DATE FILED: Jun. 30, 1986

14. 4,928,225, May 22, 1990, Coherent cache structures and methods; Daniel M. McCarthy, et al., 364/200, 228.1, 228.3, 243, 243.4, 243.41

[IMAGE AVAILABLE]

US PAT NO: 4,928,225 [IMAGE AVAILABL] L7: 14 of 27
DATE FILED: Sep. 2, 1988

15. 4,912,632, Mar. 27, 1990, Memory control subsystem; Alain Gach, et al., 364/200, 221, 221.1, 228.1, 229, 229.2, 230, 230.2, 238.3, 238.4, 239, 239.7, 241.2, 242.3, 242.31, 242.6, 242.91, 243, 243.4, 243.41, 247, 247.4, 254, 254.3, 260, 260.3, 265, 265.1, 265.3 [IMAGE AVAILABLE]

US PAT NO: 4,912,632 [IMAGE AVAILABLE] L7: 15 of 27
DATE FILED: Mar. 31, 1988

16. 4,858,111, Aug. 15, 1989, Write - back cache system using concurrent address transfers to setup requested address in main memory before dirty miss signal from cache; Steven C. Steps, 364/200, 238.3, 238.6, 239.5, 243, 243.4, 243.41, 247, 247.4, 259.2, 263 [IMAGE AVAILABLE]

US PAT NO: 4,858,111 [IMAGE AVAILABLE] L7: 16 of 27
DATE FILED: Oct. 20, 1986

17. 4,811,203, Mar. 7, 1989, Hierarchial memory system with separate criteria for replacement and writeback without replacement; James R. Hamstra, 364/200, 228.3, 238.4, 239, 239.4, 240, 240.2, 241.2, 241.4, 241.6, 242.6, 242.8, 242.91, 243, 243.4, 243.41, 244, 244.3, 244.6, 246, 246.1, 246.11, 246.12, 246.3, 246.5, 247, 248.1, 251, 251.3, 251.5, 254, 254.5, 254.6, 255.1, 255.2, 255.7, 259, 259.5, 259.6, 260, 260.1, 264, 264.6, 268, 268.3, 268.8, 268.9, 269.3, 271.9, 273.4 [IMAGE AVAILABLE]

US PAT NO: 4,811,203 [IMAGE AVAILABLE] L7: 17 of 27
DATE FILED: Mar. 3, 1982

18. 4,794,521, Dec. 27, 1988, Digital computer with cache capable of concurrently handling multiple accesses from parallel processors; Michael L. Ziegler, et al., 364/200, 228.1, 228.2, 228.7, 228.9, 232.21, 243, 243.4, 243.41, 243.44, 243.6, 246, 246.3, 246.4, 247, 247.2, 247.3, 254, 254.3, 254.4, 256.3, 256.4, 258, 258.1, 258.2, 258.3, 258.4, 261.3, 261.6, 262, 262.1, 262.4, 262.8, 264, 264.1, 271.5, 280, 280.2, 281.3, 281.4, 281.7 [IMAGE AVAILABLE]

US PAT NO: 4,794,521 [IMAGE AVAILABLE] L7: 18 of 27
DATE FILED: Jul. 22, 1985

19. 4,783,736, Nov. 8, 1988, Digital computer with multisection cache; Michael L. Ziegler, et al., 364/200, 228.3, 229, 229.2, 230, 230.1, 231.9, 234, 243, 243.4, 246, 246.4, 263 [IMAGE AVAILABLE]

US PAT NO: 4,783,736 [IMAGE AVAILABLE] L7: 19 of 27
DATE FILED: Jul. 22, 1985

20. 4,725,945, Feb. 16, 1988, Distributed cache in dynamic rams; Eric P. Kronstadt, et al., 364/200; 365/230.03, 230.08, 238.5 [IMAGE AVAILABLE]

US PAT NO: 4,725,945 [IMAGE AVAILABLE] L7: 20 of 27
DATE FILED: Sep. 18, 1984

21. 4,700,330, Oct. 13, 1987, Memory for a digital data processing system including circuit for controlling refresh operations during power-up and power-down conditions; Barbara H. Altman, et al., 365/222; 364/900, 926.92, 948.5, 964.9 [IMAGE AVAILABLE]

US PAT NO: 4,700,330 [IMAGE AVAILABLE] L7: 21 of 27
DATE FILED: Oct. 30, 1985

22. 4,577,293, Mar. 18, 1986, Distributed, on-chip cache; Richard E.

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erasable contactless EEPROM; Manzur Gill, et al., 365/185; 357/23.5

US PAT NO: 5,060,195 L4: 1 of 36
DATE FILED: Oct. 11, 1990

ABSTRACT:
An electrically-erasable, electrically-programmable, read-only memory cell array is formed in pairs at a face of a semiconductor substrate (11). Each memory cell includes a source region (14a) and a shaped drain region (16), with at corresponding channel region (18a) in between. A Fowler-Nordheim tunnel window subregion (15a) of the source region (14a) is located opposite the channel (18a). A floating gate conductor (FG) includes a channel section (32a) and a tunnel window section (34a). The floating gate conductor is formed in two stages, the first stage forming the channel section (32a) from a first-level polysilicon (P1A). This floating gate channel section (32a/P1A) is used as a self-alignment implant mask for the source (14a) and drain (16) regions, such that the channel junction edges are aligned with the coresponding edges of the channel section. A control gate conductor (CG) is disposed over the floating gate conductor (FG), insulated by an intervening interlevel dielectric (ILD). The memory cell is programmed by hot carrier injection from the channel (18a) to the floating-gate channel section (32a), and erased by Fowler-Nordheim tunneling from the floating-gate tunnel window section (34a) to the tunnel window subregion (15a).

2. 5,057,886, Oct. 15, 1991, Non-volatile memory with improved coupling between gates; Bert R. Riemenschneider, et al., 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

US PAT NO: 5,057,886 [IMAGE AVAILABLE] L4: 2 of 36
DATE FILED: Dec. 21, 1988

ABSTRACT:
A non-volatile memory is provided which provides a floating gate (42) disposed over control gate (38) in order to increase the coupling therebetween. The degree of coupling may be varied by adjusting the area of the floating gate formed over the control gate relative to the area of the floating gate over the substrate.

3. 5,051,793, Sep. 24, 1991, Coplanar flash EPROM cell and method of making same; Samuel T. Wang, 357/23.5, 23.1, 23.14, 54 [IMAGE AVAILABLE]

US PAT NO: 5,051,793 [IMAGE AVAILABLE] L4: 3 of 36
DATE FILED: Mar. 27, 1989

ABSTRACT:
A flash EPROM cell is fabricated using a standard two polysilicon enhancement mode n-channel transistor process. An active transistor region is formed in a silicon substrate by growing a field oxide around the region. A first polysilicon layer is deposited, etched, and oxidized to form an insulated control gate electrode. A second polysilicon layer is deposited over the active transistor region and the control gate electrode and then anisotropically etched to remove all of the second polysilicon material except for a filament adjacent to the control gate electrode. The filament can be on one side of the control gate electrode or on opposing sides of the control gate electrode. Source and drain regions are formed in the active transistor region with the control gate electrode and the floating gate electrode positioned over the channel region interconnecting the source and drain regions. Two dopants (arsenic and phosphorus) are introduced into the source and drain regions with

the floating gate electrode. The arsenic and phosphorus form n+ and n.sup.- regions, respectively, in the source and drain regions thereby permitting higher gate-assisted avalanche breakdown in erasing the floating gate electrode. The cell is programmed by hot electron channel current injection by proper voltage biasing of the control gate and drain. The resulting cell structure can be either symmetrical or asymmetrical depending on the configuration of the floating gate filament.

4. 5,050,125, Sep. 17, 1991, Electrically erasable programmable read-only memory with NAND cellstructure; Masaki Momodomi, et al., 365/185, 189.09, 189.11 [IMAGE AVAILABLE]

US PAT NO: 5,050,125 [IMAGE AVAILABLE] L4: 4 of 36
DATE FILED: Nov. 17, 1988

ABSTRACT:
An erasable programmable read-only memory with a NAND cell structure including NAND cell blocks, each of which has a selection transistor connected to the corresponding bit line and memory cell transistors connected is series. Word lines are connected to control gates of the cell transistors. In a data write mode, a selection transistor of a certain cell block containing a selected cell is rendered conductive to connect the cell block to the corresponding bit line. A control circuit is provided for applying an "L" Level voltage (approximately 0 V) to a word line connected to the selected cell, applying an "H" level voltage (approximately 20 V) to a word line or word lines positioned between the selected word line and a contact node connecting the cell block and a specific bit line associated therewith, applying a voltage corresponding to data to be written to the specific bit line, and applying an intermediate voltage between the "H" and "L" level voltages to non-selected bit lines, thereby writing the data in the selected cell by tunneling. If the data is logic "0" data, the intermediate voltage is applied also to the specific bit line.

5. 5,049,515, Sep. 17, 1991, Method of making a three-dimensional memory cell with integral select transistor; Jyh-Cherng J. Tzeng, 437/43, 38, 51, 52, 191, 193, 228, 233, 235 [IMAGE AVAILABLE]

US PAT NO: 5,049,515 [IMAGE AVAILABLE] L4: 5 of 36
DATE FILED: Jun. 22, 1990

ABSTRACT:
A three-dimensional floating gate memory cell including an integral select gate transistor is disclosed. Source and drain are formed in a silicon substrate wherein the drain is formed under a slot which has been etched into the body of the substrate. In this way, the channel defined between the source and drain has both horizontal and vertical regions. The cell also includes a floating gate, which is completely surrounded with insulation, and a control gate which is insulated above and extends over the floating gate. The control gate is also insulated above and extends over the vertical portion of the channel within the slot. This allows the second gate member to regulate the current flowing in the vertical portion of the channel; that is, the second gate member and the vertical channel section form an integral select device.

6. 5,043,940, Aug. 27, 1991, Flash EEPROM memory systems having multistate storage cells; Eliyahou Harari, 365/168, 185, 218 [IMAGE AVAILABLE]

US PAT NO: 5,043,940 [IMAGE AVAILABLE] L4: 6 of 36
DATE FILED: Jul. 17, 1989

ABSTRACT:
A memory system made up of electrically programmable read only memory

(EEPROM) cells. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems.

7. 5,041,886, Aug. 20, 1991, Nonvolatile semiconductor memory device and manufacturing method thereof; Soo-Cheol Lee, 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

US PAT NO: 5,041,886 [IMAGE AVAILABLE] L4: 7 of 36
DATE FILED: Sep. 25, 1989

ABSTRACT:
A nonvolatile semiconductor memory device is provided including a doped semiconductor substrate and three gate conductor layers electrically insulated from each other in the cell area on the substrate. A first floating gate conductor layer is formed on the substrate and covered by a second control gate conductor layer, forming a twofold polycrystalline silicon structure. A third select gate conductor layer is formed along one side wall of the twofold structure of the floating gate and control gate conductor layers, having a side wall spacer structure. The first conductor layer serves as a floating gate; the second conductor layer serves as a control gate; and the third conductor layer serves as a select gate. A field oxide layer is provided to separate cells from each other. The control and the select gates are connected in a region between cells through the field oxide layer. By providing the third conductor in the form of a side wall spacer, the cell area can be greatly reduced.

8. 5,040,134, Aug. 13, 1991, Neural network employing leveled summing scheme with blocked array; Chin S. Park, 364/602; 307/201; 364/513; 365/49, 185; 382/30, 33 [IMAGE AVAILABLE]

US PAT NO: 5,040,134 [IMAGE AVAILABLE] L4: 8 of 36
DATE FILED: May 26, 1989

ABSTRACT:
A novel associative network architecture is described in which a neural network is subdivided into a plurality of smaller blocks. Each block comprises an array of pattern matching cells which is used for calculating the relative match, or Hamming distance, between an input pattern and a stored weight pattern. The cells are arranged in columns along one or more local summing lines. The total current flowing along the local summing lines for a given block corresponds to the match for that block. Each of the blocks are coupled together using a plurality of global summing lines. The global summing lines sum the individual current contributions from the local summing lines of each associated block. Coupling between the local column lines and the global summing lines is achieved by using a specialized coupling device which permits control of the coupling ratio between the lines. By selectively turning on or off various blocks a measure of the match for individual blocks or for groups of blocks representing a subset of the network, may be calculated. Control over the coupling ratio within the blocks also prevents destructive levels of current from building up on the global summing lines.

9. 5,039,941, Aug. 13, 1991, Voltage threshold measuring circuit; Hernan A. Castro, 324/158T, 158D [IMAGE AVAILABLE]

US PAT NO: 5,039,941 [IMAGE AVAILABLE] L4: 9 of 36
DATE FILED: Jul. 27, 1990

ABSTRACT:
A circuit for determining the voltage threshold of a field-effect device

is described. The invention includes an amplifier means which produces an output voltage directly proportional to the current flowing within the device-under-test. A circuit means is utilized for receiving the output voltage from the amplifier means and for generating a feedback voltage at the gate of the field-effect device. This feedback voltage is dynamically limited by an RC time constant such that the feedback voltage rapidly settles to the voltage threshold of the field-effect device.

10. 5,036,378, Jul. 30, 1991, Memory device; Chih-Yuan Lu, et al., 357/23.5, 23.11, 41, 42, 46, 59; 365/185 [IMAGE AVAILABLE]

US PAT NO: 5,036,378 [IMAGE AVAILABLE] L4: 10 of 36
DATE FILED: Nov. 1, 1989

ABSTRACT:
A compact, high speed EEPROM is disclosed. The design features mirror-image pairs of cells with a common junction buried under a thick oxide. The oxide also supports a portion of the control and floating gates. A single erase gate, also above the oxide, is capable of erasing two rows of cells at once. Each cell also has a second junction which contacts the semiconductor substrate surface. The second junction has a conductive landing pad which facilitates small cell size.

11. 5,033,023, Jul. 16, 1991, High density EEPROM cell and process for making the cell; Steve K. Hsia, et al., 365/185; 357/23.5; 365/104, 238.5 [IMAGE AVAILABLE]

US PAT NO: 5,033,023 [IMAGE AVAILABLE] L4: 11 of 36
DATE FILED: Apr. 8, 1988

ABSTRACT:
Disclosed is a stacked gate electrically erasable programmable read only memory EEPROM cell which utilizes a floating region and a common pass transistor to provide a cell which is programmable at a relatively low drain voltage and which, in addition, by utilizing a pass transistor, overcomes the programming disturbance and false read problems associated with typical stacked gate memory cells. The cell is constructed such that programming and erasing functions take place at separate locations in the gate oxide. An EEPROM memory cell array, utilizing the above memory cell, is disclosed which provides the ability to achieve both byte erase and block erase as well as byte write capability. Also disclosed is a process for producing such a memory cell and memory array.

12. 5,029,139, Jul. 2, 1991, Word erasable buried bit line EEPROM; James L. Paterson, 365/218, 185, 238.5 [IMAGE AVAILABLE]

US PAT NO: 5,029,139 [IMAGE AVAILABLE] L4: 12 of 36
DATE FILED: Jul. 19, 1989

ABSTRACT:
An EEPROM circuit having a word-erase capability is disclosed using buried bit line fabrication techniques. The word-erasable EEPROM uses minimum additional chip area and minimum fabrication process modification.

13. 5,028,553, Jul. 2, 1991, Method of making fast, trench isolated, planar flash EEPROMS with silicided bitlines; Agerico L. Esquivel, et al., 437/43; 148/DIG.147; 437/49, 200 [IMAGE AVAILABLE]

US PAT NO: 5,028,553 [IMAGE AVAILABLE] L4: 13 of 36
DATE FILED: Jun. 5, 1990

ABSTRACT:
A non-volatile cross-point memory cell [illegible]ay comprises a trench isolated cross-point array of memory cells (10), [illegible]ich are electrically programmable and electrically FLASH eraseable, having diffused regions

plurality of control gates (54) operable as wordlines. The diffused regions (28) undergo a silicidation process to decrease their resistivity, and thereby increase the speed of the memory cell array. A tunnel oxide (18) is provided for electrical erasing and programming. Planarized, high quality insulating regions (40, 36), such as dichlorosilane oxide, buttress the floating gate (20) to isolate the bitlines from the wordlines and to improve isolation between the pass gate and the floating gate. A planar structure of the memory cell (10) provides flat topography ideal for three dimensional stacked structures. Trench isolation regions (56) reduce bitline capacitance, thereby increasing programming speed.

14. 5,019,879, May 28, 1991, Electrically-flash-erasable and electrically-programmable memory storage devices with self aligned tunnel dielectric area; Te-Long Chiu, 357/23.5; 365/185; 437/43, 44 [IMAGE AVAILABLE]

US PAT NO: 5,019,879 [IMAGE AVAILABLE] L4: 14 of 36
DATE FILED: Mar. 15, 1990

ABSTRACT:
The flash EEPROM memory device with the floating gate that is over the channel area and insulated from the channel by 200 to 1000 A of gate oxide, and that is also over the thin tunnel dielectric area at the source and insulated from the source by 70 A to 200 A of tunnel dielectric. Another improvement of the proposed version of the flash EEPROM memory device is that the tunnel dielectric area is small and self aligned to the floating gate.

15. 5,017,980, May 21, 1991, Electrically-erasable, electrically-programmable read-only memory cell; Manzur Gill, et al., 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

US PAT NO: 5,017,980 [IMAGE AVAILABLE] L4: 15 of 36
DATE FILED: Mar. 15, 1990

ABSTRACT:
An electrically-erasable, programmable ROM cell, or an EEPROM cell, is constructed using an enhancement transistor merged with a floating-gate transistor, where the floating-gate transistor has a small tunnel window, in a contact-free cell layout, enhancing the ease of manufacture and reducing cell size. The bitlines and source/drain regions are buried beneath relatively thick silicon oxide, which allows a favorable ratio of control gate to floating gate capacitance. Programming and erasure are provided by the tunnel window area, which is located near or above the channel side of the source. The window has a thinner dielectric than the remainder of the floating gate, to allow Fowler-Nordheim tunneling. By using dedicated drain or ground lines, rather than a virtual-ground layout, and by using thick oxide for isolation between bitlines, the floating gate can extend onto adjacent bitlines and isolation area, resulting in a favorable coupling ratio. Isolation between cells in the wordline direction is by a self-aligned implanted region, in this embodiment.

16. 5,012,307, Apr. 30, 1991, Electrically-erasable, electrically-programmable read-only memory; Manzur Gill, et al., 357/23.5, 54; 365/185 [IMAGE AVAILABLE]

US PAT NO: 5,012,307 [IMAGE AVAILABLE] L4: 16 of 36
DATE FILED: Mar. 15, 1990

ABSTRACT:
An electrically-erasable, programmable ROM cell, or an EEPROM cell, is constructed using an enhancement transistor merged with a floating-gate transistor, where the floating-gate transistor has a small tunnel window,

reducing cell size. The bitlines and source/drain regions are buried beneath relatively thick silicon oxide, which allows a favorable ratio of control gate to floating gate capacitance. Programming and erasing are provided by the tunnel window are near or above the channel side of the source. The window has a thinner dielectric than the remainder of the floating gate, to allow Fowler-Nordheim tunneling. By using dedicated drain or ground lines, rather than a virtual-ground layout, and by using thick oxide for isolation between bitlines, the floating gate can extend onto adjacent bitlines and isolation area, resulting in a favorable coupling ratio. Isolation between wordlines is also by thick thermal oxide in a preferred embodiment, further improving the coupling ratio. Bitline and wordline spacing may be selected for optimum pitch or aspect ratio. Bitline to substrate capacitance is minimized.

17. 5,010,028, Apr. 23, 1991, Method of making hot electron programmable, tunnel electron erasable contactless EEPROM; Manzur Gill, et al., 437/43, 49, 52, 195 [IMAGE AVAILABLE]

US PAT NO: 5,010,028 [IMAGE AVAILABLE] L4: 17 of 36
DATE FILED: Dec. 29, 1989

ABSTRACT:
An electrically-erasable, electrically-programmable, read-only memory cell array is formed in pairs at a face of a semiconductor substrate (11). Each memory cell includes a source region (14a) and a shared drain region (16), with a corresponding channel region (18a) in between. A Fowler-Nordheim tunnel window subregion (15a) of the source region (14a) is located opposite the channel (18a). A floating gate conductor (FG) includes a channel section (32a) and a tunnel window section (34a). The floating gate conductor is formed in two stages, the first stage forming the channel section (32a) from a first-level polysilicon (P1A). This floating gate channel section (32a/P1A) is used as a self-alignment implant mask for the source (14a) and drain (16) regions, such that the channel junction edges are aligned with the corresponding edges of the channel section. A control gate conductor (CG) is disposed over the floating gate conductor (FG), insulated by an intervening interlevel dielectric (ILD). The memory cell is programmed by hot carrier injection from the channel (18a) to the floating-gate channel section (32a), and erased by Fowler-Nordheim tunneling from the floating-gate tunnel window section (34a) to the tunnal window subregion (15a).

18. 5,008,212, Apr. 16, 1991, Selective asperity definition technique suitable for use in fabricating floating-gate transistor; Teh-yi J. Chen, 437/43, 52, 193, 195, 228, 233 [IMAGE AVAILABLE]

US PAT NO: 5,008,212 [IMAGE AVAILABLE] L4: 18 of 36
DATE FILED: Dec. 12, 1988

ABSTRACT:
In a semiconductor fabrication technique, a first patterned layer (16) of nonmonocrystalline semiconductor material is created on a substructure (10, 12, 14). An insulating layer (22) is thermally grown along the patterned layer in such a way that the upper edge of the remainder (16A) of the patterned layer forms an asperity (24). A blanket layer 26, preferably consisting of nonmonocrystalline semiconductor material, is formed over the insulating layer. Using an etchant that attacks the blanket and patterned layers more than the insulating layer, a selective etch is performed to remove a section of the blanket layer. The etch is continued past the blanket layer to remove the underlying portion of the insulating layer located along the asperity and then, importantly, to remove the so exposed part of the asperity. The remainder (26A) of the blanket overlies the remainder ((24A) of the asperity. The technique is particularly useful in manufacturing a [redacted]ating-gate FET for an electrically erasable programmable dev[redacted]. The remainder of the asperity facilitates tunneling during erasure.

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1. 5,048,022, Sep. 10, 1991, Memory device with transfer of ECC signals on time division multiplexed bidirectional lines; Thomas D. Bissett, et al., 371/40.1, 68.3 [IMAGE AVAILABLE]

2. 5,023,934, Jun. 11, 1991, Apparatus and method for communication of visual graphic data with radio subcarrier frequencies; Jesse Wheeless, 455/45, 23, 54, 72 [IMAGE AVAILABLE]

3. 5,014,235, May 7, 1991, Convolution memory; Steven G. Morton, 364/900, 754, 923.5, 927.8, 939.3 [IMAGE AVAILABLE]

4. 5,005,174, Apr. 2, 1991, Dual zone, fault tolerant computer system with error checking in I/O writes; William F. Bruckert, et al., 371/68.3; 364/200, 268.3 [IMAGE AVAILABLE]

5. 4,996,697, Feb. 26, 1991, Deglitching means for digital communication systems; David N. Critchlow, et al., 375/104; 455/223 [IMAGE AVAILABLE]

6. 4,994,802, Feb. 19, 1991, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 341/122, 155 [IMAGE AVAILABLE]

7. 4,953,931, Sep. 4, 1990, CPU socket supporting socket-to-socket optical communications; Bernard Ramsey, et al., 359/118; 357/40; 359/154; 385/147 [IMAGE AVAILABLE]

8. 4,943,983, Jul. 24, 1990, Subscriber unit for wireless digital telephone system; David N. Critchlow, 375/84, 8, 56, 67 [IMAGE AVAILABLE]

9. 4,933,846, Jun. 12, 1990, Network communications adapter with dual interleaved memory banks servicing multiple processors; Donald J. Humphrey, et al., 364/200, 231.4, 238.5, 240, 240.1, 242.94, 242.95, 243, 243.6, 246.4, 270, 271.4; 370/85.1 [IMAGE AVAILABLE]

10. 4,916,704, Apr. 10, 1990, Interface of non-fault tolerant components to fault tolerant system; William F. Bruckert, et al., 371/68.3, 9.1

11. 4,907,228, Mar. 6, 1990, Dual-rail processor with error checking at single rail interfaces; William F. Bruckert, et al., 364/900 [IMAGE AVAILABLE]

12. 4,905,196, Feb. 27, 1990, Method and storage device for saving the computer status during interrupt; Hubert Kirrmann, 365/200, 75 [IMAGE AVAILABLE]

13. 4,893,317, Jan. 9, 1990, Digital signals and frequency correction in

19. 4,998,220, Mar. 5, 1991, EEPROM with improved erase structure; Boaz Eitan, et al., 365/185; 357/23.5; 365/[redacted]218 [IMAGE AVAILABLE]

US PAT NO: 4,998,220 [IMAGE AVAILABLE] L4: 19 of 36
DATE FILED: May 3, 1988

ABSTRACT:
An electrically erasable programmable read only memory (EEPROM) constructed in accordance with the invention includes a source, a drain, a channel region formed between the source and drain, a floating gate extending over a first portion of the channel region but not a second portion of the channel region, and a control gate extending over a first portion of the floating gate and the second portion of the channel region. Of importance, the EEPROM includes an erase gate which is formed concurrently with the control gate and extending over a second portion of the floating gate. Because the erase gate is formed concurrently with the control gate, the process used to form the EEPROM requires only two layers of polysilicon. Also, because electrons tunnel between the floating gate and the erase gate during electrical erase instead of between the floating gate and the drain, there is no PN junction breakdown during electrical erase and therefore, the EEPROM array can be erased using a low current voltage supply.

20. 4,996,668, Feb. 26, 1991, Erasable programmable memory; James L. Paterson, et al., 365/185; 357/23.5; 365/189.01, 230.01 [IMAGE AVAILABLE]

US PAT NO: 4,996,668 [IMAGE AVAILABLE] L4: 20 of 36
DATE FILED: Feb. 20, 1990

ABSTRACT:
EEPROM memories with crosspoint cells using buried source and drain lines plus merged floating gate transistors with floating gate coupling to control gate over the buried line insulator for high packing plus low voltage operation.

21. 4,994,403, Feb. 19, 1991, Method of making an electrically programmable, electrically erasable memory array cell; Manzur Gill, 437/43; 357/23.5; 437/48, 49, 50, 52, 61 [IMAGE AVAILABLE]

US PAT NO: 4,994,403 [IMAGE AVAILABLE] L4: 21 of 36
DATE FILED: Dec. 28, 1989

ABSTRACT:
A pair of electrically erasable, electrically programmable memory cells are formed at a face of a semiconductor layer (10) and include respective drain regions (30a, 30b), a shared source region (28) and respective channel regions (38a, 38b). Each cell has a floating gate conductor (46a, 46b) which may be programmed by hot electron injection and erased by Fowler-Nordheim electron tunneling through respective tunneling oxide windows (40a, 40b) overlying a portion of source region (28) adjacent respective channels (38a, 38b). A wordline or control gate conductor (62) is insulatively disposed adjacent the floating gates (46a, 46b) to program or erase.

22. 4,970,692, Nov. 13, 1990, Circuit for controlling a flash EEPROM having three distinct modes of operation by allowing multiple functionality of a single pin; Syed Ali, et al., 365/218, 189.01, 189.03, 189.05, 230.02, 230.06 [IMAGE AVAILABLE]

US PAT NO: 4,970,692 [IMAGE AVAILABLE] L4: 22 of 36
DATE FILED: Feb. 20, 1990

ABSTRACT:
An EEPROM receives a first address from a microprocessor. If the first address equals a first predetermined value, the EEPROM goes into a

voltage operation.

30. 4,894,802, Jan. 16, 1990, Nonvolatile memory cell for eeprom including a floating gate to drain tunnel area positioned away from the channel region to prevent trapping of electrons in the gate oxide during cell erase: Steve K. Hsia, et al., 365/185; 357/23.5; 365/182

US PAT NO: 4,894,802 L4: 30 of 36
DATE FILED: Feb. 2, 1988

ABSTRACT:
Disclosed is a nonvolatile memory cell which utilizes a tunnel window to discharge the floating gate at a location spacially displaced from the program path for the cell. Also disclosed is a process for making such a memory cell.

31. 4,888,735, Dec. 19, 1989, ROM cell and array configuration; Wung K. Lee, et al., 365/185, 104

US PAT NO: 4,888,735 L4: 31 of 36
DATE FILED: Apr. 28, 1988

ABSTRACT:
An EPROM structure incorporating Vss isolation transistors having gates on wordlines shared by respective rows of conventional self-aligned EPROM cells, and having source and drain regions connected in series between EPROM cell source regions and the ground Vss terminal. An isolation transistor becomes conductive only when an EPROM cell sharing its wordline is selected. During programming, otherwise possible leakage current through unselected cells sharing the selected bitline is blocked by the Vss isolation transistor. Only one unselected adjacent cell, which shares a common source region with the selected cell, can leak. This leakage, if properly suppressed and compensated, has no disturbance on the unselected or selected cells during array programming. The EPROM cell drain punchthrough voltage and channel length can thus be reduced to obtain ROM and EPROM cells with low threshold voltages, low drain programming voltages, short programming times, low cell junction and bitline capacitances, and high read currents. EPROM-type products can be constructed with single low power supplies, on-chip high voltage pumping and high speed read and programming. Additional rows of shared isolation transistors can be formed by adding extra poly(2) lines in parallel to the wordlines betwen EPROM source diffusions to achieve fuller programming isolation. This cell and array isolation configuration can be extended to flash EEPROM type products. The cell and array configuration of the present invention can also be embodied in ROM type products by omitting the poly(1) floating gates underneath the poly(2) worlines in ROM cells.

32. 4,888,734, Dec. 19, 1989, EPROM/ flash EEPROM cell and array configuration; Wung K. Lee, et al., 365/185, 104

US PAT NO: 4,888,734 L4: 32 of 36
DATE FILED: Dec. 28, 1987

ABSTRACT:
An EPROM structure incorporating Vss isolation transistors having gates on wordlines shared by respective rows of conventional self-aligned EPROM cells, and having source and drain regions connected in series between EPROM cell source regions and the ground Vss terminal. An isolation transistor becomes conductive only when an EPROM cell sharing its wordline is selected. During programming, otherwise possible leakage current through unselected cells sharing the selected bitline is blocked by the Vss isolation transistor. Only one unselected adjacent cell, which shares a common source region with the selected cell, can leak. This leakage, if properly suppressed and compensated, has no disturbance on

electrodes (40) extend over tunnel windows (22) that are formed on the semiconductor layer (10) in positions adjacent a single erase region (54). An integral contact (64) is made through multilevel oxide (56, 58) from a metal erase line (70) to each erase region (54).

36. 4,780,750, Oct. 25, 1988, Electrically alterable non-volatile memory device; Joseph G. Nolan, et al., 357/23.5, 12, 23.6, 41, 54; 365/185

US PAT NO: 4,780,750 L4: 36 of 36
DATE FILED: Jan. 3, 1986

ABSTRACT:
In this invention, an Electrically Alterable Non-Volatile Memory (EANOM) cell is disclosed. The EANOM cell comprises an MOS transistor, having a source, a gate and a drain. The EANOM cell also has a two-terminal tunnel device, one end of which is connected to the gate of the MOS transistor. The other terminal being labelled "T". The tunnel device causes charges to be stored or removed from the gate of the MOS transistor. In a preferred embodiment, a four-terminal EANOM cell is disclosed. The four terminals of the EANOM cell are terminals T, S (source of the MOS transistor), D (drain of the MOS transistor) and a terminal C which is capacitively coupled to the gate of the MOS transistor. The EANOM cell can be used in a memory circuit to increase the reliability thereof. Two or more EANOM cells are connected in tandem and operate simultaneously. Catastrophic failure of one EANOM cell results in an open circuit with the other EANOM cell continuing to function.

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1. 5,043,940, Aug. 27, 1991, Flash EEPROM memory systems having multistate storage cells; Eliyahou Harari, 365/168, 185, 218 [IMAGE AVAILABLE]

US PAT NO: 5,043,940 [IMAGE AVAILABLE] L5: 1 of 1
DATE FILED: Jul. 17, 1989

ABSTRACT:
A memory system made up of electrically programmable read only memory (EPROM) or flash electrically erasable and programmable read only memory (EEPROM) cells. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnatic disk storage devices in computer systems.

Planar ready high quality insulating regions (40, 36), such as dichlorosilane oxide, buttress the floating gate (20) to isolate the bitlines form the wordlines and to improve isolation between the pass gate and the floating gate. A planar structure of the memory cell (10) provides flat topography ideal for three dimensional stacked structures. Trench isolation regions (56) reduce bitline capacitance, thereby increasing programming speed.

26. 4,949,309, Aug. 14, 1990, EEPROM utilizing single transistor per cell capable of both byte erase and flash erase; Kamesawara K. Rao, 365/218; 307/465; 357/23.5; 365/104, 185 [IMAGE AVAILABLE]

US PAT NO: 4,949,309 [IMAGE AVAILABLE] L4: 26 of 36
DATE FILED: May 11, 1988

ABSTRACT:
An array of floating gate transistors is connected so that some of the floating gate transistors within the array can be erased without affecting the state of other floating gate transistors within the array, or in the alternative, the entire array of floating gate transistors can be erased simultaneously.

27. 4,933,906, Jun. 12, 1990, Non-volatile semiconductor memory device; Yasushi Terada, et al., 365/208, 204, 230.03 [IMAGE AVAILABLE]

US PAT NO: 4,933,906 [IMAGE AVAILABLE] L4: 27 of 36
DATE FILED: Nov. 18, 1988

ABSTRACT:
A semiconductor memory device of erasable programmable rear only memory type is disclosed the memory device has a pair of memory cell arrays between which a differential amplifier is provided. Each of the memory cell arrays has a current-to-voltage converter circuit associated therewith. When a memory cell in either one of the pair of memory cell array is selected, a bit line being coupled to the selected memory cell is charged by one current-voltage conversion circuit, while at the same time at least one bit line in the other memory cell array where no memory cell has been selected is charged by the associated current-voltage converter circuit at arrayed different from the bit line coupled to the selected memory cell. A differential amplifier senses and amplifies a potential difference between the charged bit lines to provide a high speed read-out of the memory device.

28. 4,924,437, May 8, 1990, Erasable programmable memory including buried diffusion source/drain lines and erase lines; James L. Paterson, et al., 365/185; 357/23.5; 365/218; 437/43 [IMAGE AVAILABLE]

US PAT NO: 4,924,437 [IMAGE AVAILABLE] L4: 28 of 36
DATE FILED: Dec. 9, 1987

ABSTRACT:
An EEPROM cell and array of cells is disclosed having buried diffusion source/drain lines and buried diffusion erase lines. The cells further include coupling between the floating gate and control gate above the source/drain diffusion. The disclosed cell allows high packing density and operation at low voltages.

29. 4,912,676, Mar. 27, 1990, Erasable programmable memory; James L. Paterson, et al., 365/185; 357/23.5; 365/184, 189.01, 230.01

US PAT NO: 4,912,676 L4: 29 of 36
DATE FILED: Aug. 9, 1988

ABSTRACT:
EEPROM memories with crosspoint cells using buried source and drain lines plus merged floating gate transistors with floating gate coupling to

a group of condensers and contains all records contained in all condensers under its supervision. All information can be uploaded from condensers to subhost or downloaded from subhost to condenser. In case of any failure in any subsystem, all lower level systems continue to operate. All controllers are interchangeable.

3. 4,817,091, Mar. 28, 1989, Fault-tolerant multiprocessor system; James A. Katzman, et al., 371/9.1; 364/200, 229, 229.2, 229.4, 230, 230.3, 232.7, 232.8, 235, 236.2, 236.3, 237, 238.3, 238.4, 239, 239.1, 239.6, 240, 240.2, 240.5, 240.8, 240.9, 241.9, 244, 244.3, 246, 246.3, 247, 247.7, 249, 251, 251.3, 256.3, 256.5, 260, 260.1, 262.4, 262.8, 265, 265.3, 265.4, 266.6, 267, 267.1, 267.7, 268, 268.3, 268.4, 268.7, 268.8, 268.9 , 270, 270.3, 270.5, 270.9, 271, 271.2, 271.4, 273.4 , 273.5, 280, 280.6, 281, 281.3, 281.6, 281.7, 281.8, 284, 284.3, 285, 285.3; 371/11.3, 62 [IMAGE AVAILABLE]

US PAT NO: 4,817,091 [IMAGE AVAILABLE] L6: 3 of 16

ABSTRACT:
In a multiprocessor system interconnected by a bus structure that provides communication and information transfers between the processor modules of the system, each processor broadcasts a central message to all the other processors of the system on a periodic basis. A processor module not receiving the control message from a sending processor module will assume the sending processor module has failed, and operate to take over the task of the failed processor module.

4. 4,811,203, Mar. 7, 1989, Hierarchial memory system with separate criteria for replacement and writeback without replacement; James R. Hamstra, 364/200, 228.3, 238.4, 239, 239.4, 240, 240.2, 241.2, 241.4, 241.6, 242.6, 242.8, 242.91, 243, 243.4, 243.41, 244, 244.3, 244.6, 246, 246.1, 246.11, 246.12, 246.3, 246.5, 247, 248.1, 251, 251.3, 251.5, 254, 254.5, 254.6, 255.1, 255.2, 255.7, 259, 259.5, 259.6, 260, 260.1, 264, 264.6, 268, 268.3, 268.8, 268.9 , 269.3, 271.9, 273.4 [IMAGE AVAILABLE]

US PAT NO: 4,811,203 [IMAGE AVAILABLE] L6: 4 of 16

ABSTRACT:
In a memory system having a cache memory and a bulk memory, write-back of data segments in the cache memory to the bulk memory for replacement purposes is accomplished in accordance with a least recently used algorithm while the write-back of written-to segments to the bulk memory without replacement is accomplished in accordance with an age since first write algorithm.

5. 4,807,116, Feb. 21, 1989, Interprocessor communication; James A. Katzman, et al., 364/200, 229, 229.2, 229.4, 230, 232.7, 232.9, 238.3, 238.6, 239, 239.7, 240, 240.5, 240.8, 240.9, 241, 242.6, 242.91, 244, 244.3, 244.8, 246, 246.3, 247, 251, 251.1, 256.3, 260, 260.1, 263.1, 265, 266.3, 266.5, 268, 268.3, 268.9 , 270.5, 270.7, 271, 271.2, 273, 273.4 , 273.5, 280, 281.3, 281.7, 281.8, 284, 284.1, 284.3, 284.4 [IMAGE AVAILABLE]

US PAT NO: 4,807,116 [IMAGE AVAILABLE] L6: 5 of 16

ABSTRACT:
In a multiprocessor system comprising a plurality of individual processor modules interconnected by a bus structure, including a bus controller, for providing communication between the processor modules, a method and apparatus for interprocessor communication includes one of the processor modules sending a request signal to the bus controller to request a transmission; the bus controller polling the processor modules to identify the requesting processor module; the requestor processor module responding to the poll with the identification of the receiver processor module; the bus controller interrogating the receiver processor module to

drain punchthrough voltage and channel length can thus be reduced to obtain an EPROM cell with a low threshold voltage, low drain programming voltage, short programming time, low capacitance junction and bitline capacitance, and high read current. EPROM-type products can be constructed with single low power supplies, on-chip high voltage pumping and high speed read and programming. Additional rows of shared isolation transistors can be formed by adding extra poly2 lines in parallel to the wordlines between EPROM source diffusions to achieve fuller programming isolation. This cell and array isolation configuration can be extended to flash EEPROM type products.

33. 4,861,730, Aug. 29, 1989, Process for making a high density split gate nonvolatile memory cell; Steve K. Hsia, et al., 437/43; 148/DIG.82, DIG.102; 357/23.5, 23.9, 91; 437/27, 150, 924, 984

US PAT NO: 4,861,730 L4: 33 of 36
DATE FILED: Jan. 25, 1988

ABSTRACT:
A process is disclosed for producing a high density split gate nonvolatile memory cell which includes a floating gate and a control gate that is formed above the floating gate. The drain region is self-aligned to the floating gate and the source region is self-aligned to the control gate. Fully self-aligned implantation is made possible by the process and structure using self-aligned etch. Programming of the memory cell uses standard EPROM programming, and erasing is accomplished by Fowler-Nordheim tunneling or photoemission. The memory cell can be made with a reduced cell size and read current uniformity is obtained.

34. 4,858,194, Aug. 15, 1989, Nonvolatile semiconductor memory device using source of a single supply voltage; Yasushi Terada, et al., 365/203, 189.01, 189.09, 222

US PAT NO: 4,858,194 L4: 34 of 36
DATE FILED: Feb. 10, 1988

ABSTRACT:
A nonvolatile semiconductor memory device comprises memory cells each formed of a single memory transistor and can be accessed in a bit-by-bit manner to eliminate an erase cycle in a data write cycle. The memory device comprises precharging circuits for precharging word lines and bit lines in the data write cycle, tri-level V.sub.pp switches, in response to a data to be written and an output of X decoder, for applying to a selected word line a write voltage V.sub.pp when the data to be written is "1" while a ground potential when the data to be written is "0", and further applying remaining non-selected word lines the precharge voltage, and tri-level V.sub.pp switches, in response to a data to be written and an output of Y decoder, for applying to a selected bit line the ground potential when the data to be written is "1" while the write high-voltage V.sub.pp when the data to be written is "0", and further to the remaining non-selected bit lines the precharge voltage.

35. 4,839,705, Jun. 13, 1989, X-cell EEPROM array; Howard L. Tigelaar, et al., 357/23.5, 41, 45; 365/185

US PAT NO: 4,839,705 L4: 35 of 36
DATE FILED: Dec. 16, 1987

ABSTRACT:
An X-cell EEPROM array includes a plurality of common source regions (50) that each border on four gate regions (46), both formed at a face of a semiconductor substrate (10). Each gate region (46) further adjoins a common drain region (52). Each drain region (52) is a common drain for two EEPROM select and memory transistors. A common erase region (54) is implanted into the semiconductor layer (10) in a position remote from the